A Robust DC-Link Voltage Control Strategy to Enhance the Performance of Shunt Active Power Filters Without Harmonic Detection Schemes

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***Abstract*—Shunt active power filters ($SAPFs$) implemented without harmonic detection schemes are susceptible to sudden load variations. This paper proposes a robust control strategy to reduce this drawback. In this strategy, the dc-link voltage is regulated by a hybrid control technique combining a standard proportional–integral PI and a sliding-mode (SM) controllers. The SM scheme continuously determines the gains of the PI controller based on the control loop error and its derivative. The chattering due to the SM scheme is reduced by a transition rule that fixes the controller gains when steady-state condition is reached. This controller is termed as dual-sliding-mode-proportional–integral. The phase currents of the power grid are indirectly regulated by double-sequence controllers with two degrees of freedom, where the internal model principle is employed to avoid reference frame transformation. The proposed control strategy ensures zero steady-state error and improves the performance under hard transients such as load variation. Additionally, it presents robustness when the $SAPF$ is operating under unbalanced conditions. Experimental results demonstrate the performance of the proposed control scheme.**

***Index Terms*—Adaptive control strategy, harmonic compensation, power factor correction, shunt active power filter (SAPF).**

Nomenclature

ANN	Artificial neural network.
$BEBSs$	Balanced-energy-based schemes.
DSC	Double-sequence controller.
$DSM-PI$	Dual sliding mode–proportional–integral.
DSP	Digital signal processor.
GA	Genetic algorithm.
$HEBSs$	Harmonic extractor-based strategies.
IMP	Internal model principle.
$OFLs$	Optical fiber links.
PB	Plug-in board.
PLL	Phase-locked loop.
$SAPF$	Shunt active power filter.
SM	Sliding mode.
$VS-APPC$	Variable structure–adaptive pole placement control.
VSI	Voltage source inverter.

Subscripts

d	d-axis in dq frame;
q	q-axis in dq frame;
s	refers to grid variables;
f	refers to $SAPF$ variables;
l, r	refer to load variables.

Superscripts

s	refers to dq stationary frame;
e	refers to dq rotational frame;
$+$	refers to $SM-PI$ upper switching limit;
$-$	refers to $SM-PI$ lower switching limit;
av	refers to $SM-PI$ average gains.

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I. Introduction

THE growing use of power converters as embedded devices in household, commercial, or industrial electronic-based appliances has deteriorated the power quality of the mains. Those nonlinear loads generate current harmonics and reactive power that result in voltage drops on the supply network impedance and may induce unbalance operating conditions. These effects can be even worse if the loads change randomly. Conventional solutions such as passive filters for reducing harmonic pollution are ineffective. Furthermore, the standards and recommendations that delimit the boundaries of harmonic distortion and reactive power in the power system have become more restricted [1], [2], which has stimulated the use of active power compensation [3], [4].

$SAPFs$ have been extensively used for compensation of harmonics, reactive power, negative sequences, and/or flickers [5]–[7]. The conventional control schemes applied to $SAPF$ are $HEBSs$ because their effectiveness depends on how quickly and accurately the harmonic components of the nonlinear loads are identified [8]. Harmonic extractors used in $HEBSs$ can be implemented by using different approaches such as traditional

$d-q$ method [9] and $p-q$ theory [10], adaptive filters [11], wavelet [12], GA [13], or ANN [14]. The $SAPF$ can be also implemented without the use of the load harmonic extractors. In this case, the harmonic compensating term is obtained from the system active power balance [15]–[19]. These systems can be considered as $BEBSs$, and their performance depends on how fast the system reaches the equilibrium state [17].

The control systems of $SAPF$ implemented based on $HEBS$ or $BEBS$ concepts are generally accomplished by a cascade strategy composed by an inner control loop for regulating the filter phase currents $(HEBS)$ or grid phase currents $(BEBS)$ and an outer control loop to set the dc-link voltage. The effectiveness of both solutions depends on the performance of the control loops. In the case of $HEBS$, the dc-link controller regulates the dc capacitor voltage at the suitable level to achieve the compensation objectives. Moreover, the current control loop should regulate the $SAPF$ phase currents, composed mainly of harmonic components, which requires more complex strategies for achieving suitable performance indices. As for the case when $BEBS$ is used, the dc-link controller regulates the dc capacitor voltage and ensures the system active power balance, which in turn determines the reference currents of the power grid. As the power system phase currents in steady state are basically composed of the fundamental component, the current control strategy used can be simplified. Generally, PI controllers have been used for regulating the voltage of dc-link capacitors of both approaches. However, some alternatives to enhance $SAPF$ dc-link performance have been proposed, such as the feedforward schemes for compensating the power grid voltage fluctuations [20] or the use of adaptive control techniques for flexibility of reactive compensation in hybrid active power filters [21]. Regarding the current control loop, the technique to be used depends on the methodology employed. In the case of $HEBS$, the standard solution employs PI controllers implemented in the coordinates of the grid voltage vector reference frame [22]. However, the use of these controllers results in steady-state errors, and the limitation of bandwidth has not allowed for a satisfactory harmonic compensation [23]. There are other possible solutions such as dead-beat control [24], SM control (SMC) [25], adaptive control [26], resonant control [27], and repetitive-based control [28]. Among them, the latter seems to be the most suitable in addition to having the advantage of selective harmonic compensation. However, its implementation requires a controller for the fundamental frequency and others for the remaining harmonic components, which can be quite expensive [29]. When the $SAPFs$ are implemented according to the $BEBS$ methodology, the current control strategy can be simplified by using only one resonant controller per phase, tuned at the fundamental frequency [17].

Recently, a different approach of an adaptive control strategy applied for $SAPF$ using the $BEBS$ methodology has been proposed for compensating the harmonic distortion, reactive power, and unbalanced load [17]. In this $SAPF$, the current control scheme is implemented by an adaptive pole placement control, integrated with a variable structure scheme $(VS-APPC)$. The main advantage of the proposed control strategy refers to the reduction of $SAPF$ complexity of implementation, resulting in reduced costs (because it is not necessary to have load and filter phase current measurements, thus reducing the number of current sensors), without reduction of its compensation effectiveness. However, this control scheme has a drawback that is the poor performance of the dc-link control loop during the occurrence of severe load variations.

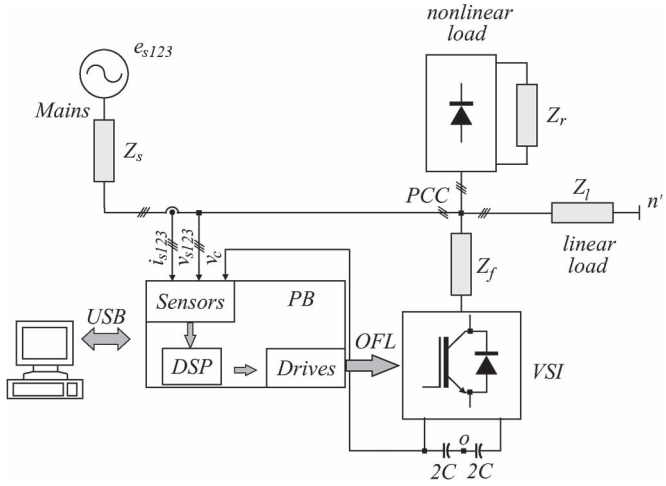


Fig. 1. Basic diagram of the proposed SAPF system.

This paper proposes a robust control strategy to improve $BEBS$ power filters during severe load changes. In this approach, the dc-link voltage is regulated by a hybrid control strategy composed by the association of a standard PI and an SM controllers. The SM scheme continuously determines the gains of the PI controller based on the control loop error and its derivative. The chattering due to the SM scheme is reduced by a transition rule that fixes the controller gains when system steady state is reached. This new controller is termed as $DSM-PI$. The grid phase currents are indirectly regulated by $DSCs$ with two degrees of freedom, where the IMP is employed to avoid reference frame transformation. These control structures ensure zero steady-state error in addition to presenting robustness to possible imbalances in the $SAPF$ system. The proposed control strategy is very suitable for sampled-data control and can be easily implemented on DSPs. The performance of the proposed control scheme is demonstrated with several experimental test results.

II. System Description and Modeling

Fig. 1 presents the topology of $SAPF$ used in the laboratory prototype. It comprises a three-phase grid source e_{s123} with its internal impedance $(Z_s = r_s + sl_s)$ that feeds a three-phase load bank consisting of parallel association of a noncontrolled rectifier and a three-phase linear load $(Z_l = r_l + sl_l)$. The $SAPF$ is implemented with a VSI connected to the PCC through inductors l_f (i.e., $Z_f = r_f + sl_f$, wherein r_f is the intrinsic resistance of l_f). The control system program is executed in a DSP linked in with a PB that handles the measurement of the variables, as well as the converter drivers via $OFLs$.

A. SAPF Grid-Tied Power Converter Modeling

The model of the $SAPF$ grid-tied power converter considering the interaction of the grid impedances to both the system

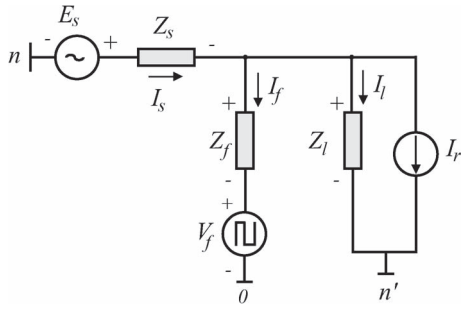


Fig. 2. Equivalent circuit of a SAPF system.

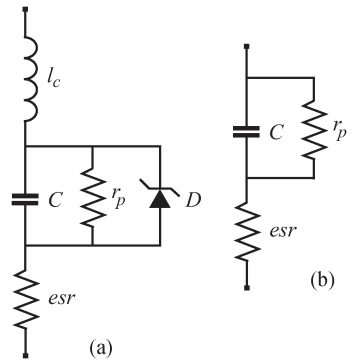


Fig. 3. Equivalent circuit of the electrolytic capacitor. (a) Manufacturer model. (b) Simplified model.

load and the filter was extensively studied in [17]. Based on this study, the system in Fig. 1 can be described by the per-phase equivalent circuit presented in Fig. 2. In this circuit, the nonlinear load is represented by a current source I_r that represents the distorting currents generated by the rectifier. From the equivalent circuit shown in Fig. 2, the transfer function representing the dynamic behavior of power grid currents can be given by

$$G_c(s) = \frac{I^{s\prime}_{sdq}(s)}{V^{s}_{fdq}(s)} \approx -\frac{b_s}{s + a_s} \tag{1}$$

where $b_s = 1/(l_f + l_s)$, and $a_s = (r_f + r_s)/(l_f + l_s)$. In this model, parameters a_s and b_s may vary as a function of either the random behavior of nonlinear load or the grid impedances. Further details on the system modeling could be found in [17].

The $SAPF$ in Fig. 1 employs aluminum electrolytic capacitors in its dc link to ensure a constant dc voltage v_C. These capacitors are submitted to high-current ripple that can lead to self-heating and consequently modify its dynamic characteristics [30]. The overall dynamic performance of the $BEBS$-based solution is entirely dependent on the ability to keep a constant dc voltage at the dc link. Therefore, for the effective control of the dc bus voltage, it is necessary to describe the dynamic model of these capacitors. Such model can be represented by different electric models [30], [31]. The model chosen in this paper is shown in Fig. 3(a). It is the same used by manufacturers and also it is described by parameters easily identifiable.

In this circuit, capacitance C decreases by increasing frequency. Resistance esr decreases by increasing frequency and temperature. Inductance l_c is relatively independent of both frequency and temperature; it increases with terminal spacing. Resistance r_p accounts for leakage current in the capacitor; it decreases by increasing capacitance, temperature, and voltage. The Zener diode D models the overvoltage and the reverse voltage behavior.

Inductance l_c has significant values when the switching frequency employed on the power converter is higher than 100 kHz. In applications with $SAPF$, the switching frequency used is far lower, and therefore, the inductance l_c can be neglected from the model. The Zener diode D is also neglected because it does not affect the linear behavior of the capacitor. Thus, the equivalent circuit of the capacitor can be reduced to the one shown in Fig. 3(b). Based on this equivalent circuit, the dynamic model of the electrolytic capacitor can be given by

$$\frac{V_C(s)}{I^{e}_{sd}(s)} = \frac{esr(s + \frac{1}{r_pC} + \frac{1}{esrC})}{s + \frac{1}{r_pC}}. \tag{2}$$

The transfer function represented by (2) has a pole that depends on the values of C and r_p and a zero depending on the values of C, r_p, and esr. Considering a reasonable case where $r_p \gg esr$, it is possible to simplify the model given by (2), neglecting the value of esr. In this case, the resulting transfer function is given by

$$G_v(s) = \frac{V_C(s)}{I^{e}_{sd}(s)} = \frac{\frac{1}{C}}{s + \frac{1}{r_pC}} = \frac{b_c}{s + a_c} \tag{3}$$

where $b_c = 1/C$, and $a_c = 1/(r_pC)$.

The dynamic behavior of both models varies depending on C, r_p, and esr, which in turn vary as a function of frequency, voltage, and temperature.

III. Control Scheme

Fig. 4 presents the block diagram of the proposed control scheme for the $SAPF$ based on the methodology. In this block diagram, the dc-link voltage is regulated by a $DSM - PI$ controller. It is done by generating the reference current i^{e*}_{sd}, which determines the system active power component. The phase angle of the power grid voltage vector θ_s is determined by using a PLL. Thus, the dq reference phase currents in a stationary reference frame dq^s can be obtained by $i^{s*}_{sd} = i^{e*}_{sd}\cos(\theta_s)$ and $i^{s*}_{sq} = i^{e*}_{sd}\sin(\theta_s)$, respectively. The reference current i^{e*}_{sd} is defined to guarantee the active power balance of the $SAPF$ system. The phase currents of the power grid are indirectly regulated by two $DSCs$, in which the IMP is employed to avoid reference frame transformations. The $DSCs$ generate proper active filter phase voltages v^{s*}_{fd} and v^{s*}_{fq}. These DSC current controllers will be described next. The unmodeled disturbances I^{s}_{edq} and $I^{s\prime}_{rdq}$ can be estimated and introduced into the algorithm of DSC current controllers. However, theoretical studies and experimental essays have shown that this control scheme has the ability of compensating such unmodeled disturbances. Block $x^{s}_{dq}/123$ performs the orthogonal transformation from the dq^s reference frame to the three-phase system, i.e., from v^{s*}_{fdq} to v^{*}_{f123}. Based on these reference voltages, a suitable PWM strategy determines the duty cycle of VSI power switches.

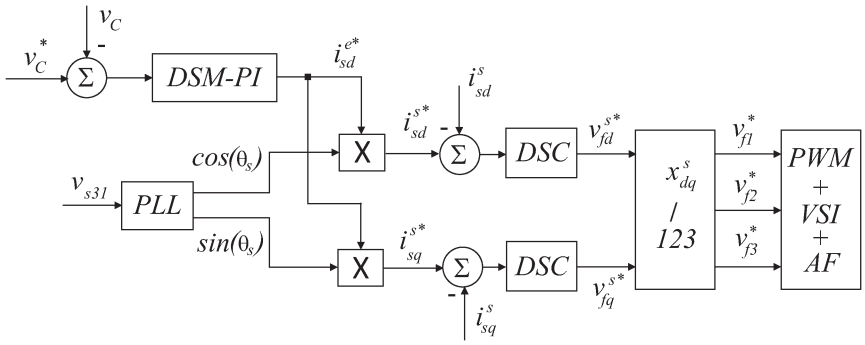


Fig. 4. Block diagram of the proposed control strategy. x^e_{dq} denotes voltage vector reference frame variables, whereas x^s_{dq} denotes stationary reference frame variables.

A. Grid Currents Control Strategy

The control strategy employed in this paper for regulating the grid currents (see block DSC in Fig. 4) is based on the double-sequence control scheme, which employs one controller for the positive sequence and another for the negative sequence [32]. Moreover, this controller has the advantage of using the IMP in its modeling that avoids the reference frame transformation while guarantees null steady-state error. Generically, the state-space model of the DSC can be represented by

$$\frac{dx^s_{1dqi}}{dt} = 2k_{ii}\varepsilon^s_{idq} + x^s_{2dqi} \tag{4}$$

$$\frac{dx^s_{2dqi}}{dt} = -\omega_s^2 x^s_{1dqi} \tag{5}$$

$$v^{s*}_{fdq} = x^s_{1dqi} + 2k_{pi}\varepsilon^s_{idq} \tag{6}$$

where k_{pi} and k_{ii} are the controller gains, and ω_s is the fundamental frequency of the power grid.

The transfer function of the current controller on the stationary reference frame can be given by

$$C_c(s) = \frac{2k_{pi}s^2 + 2k_{ii}s + 2k_{pi}\omega_s^2}{s^2 + \omega_s^2}. \tag{7}$$

The design of the DSC is achieved by using the zero-pole cancelation method. Therefore, considering that a_s can be associated to the current controller gains k_{pi} and k_{ii} as

$$a_s \approx \frac{k_{ii}}{k_{pi}} \tag{8}$$

the desired bandpass frequency of the DSC can be determined as $\omega_c = b_s k_{pi}$. Thus, it is possible to determine the controller gains as a function of a_s and b_s, which results in

$$k_{pi} = \frac{\omega_c}{b_s} \tag{9}$$

$$k_{ii} = \frac{a_s\omega_c}{b_s}. \tag{10}$$

Different design methodologies can be employed for calculating the current controller gains. Here, the proposed design approach achieves a good performance in the current control loop.

B. DC-Link Voltage Controller

The proposed control scheme for the dc link is implemented by a nonstandard robust $SM-PI$, which is implemented by a proportional–integral (PI) controller in which its controller gains are calculated by using the SMC approach based on the sliding surface composed by the control loop error and its derivative. The chattering due to the SMC scheme is reduced by a transition scheme, which fixes the controller gains when system steady state is reached. The inclusion of this transition scheme in the $SM-PI$ controller results in a new controller that is termed here as $DSM-PI$.

1) $SM-PI$ Control Scheme: Consider the dynamic model of the dc link of the $SAPF$ described by (3) with the value of esr neglected. Admitting that the $SM-PI$ controller transfer function can be written as

$$C_v(s) = \frac{\widetilde{k}_p s + \widetilde{k}_i}{s} \tag{11}$$

controller gains $\widetilde{k}_p$ and $\widetilde{k}_i$ are determined by SMC theory. The closed-loop dynamics of the dc-link voltage can be described as follows:

$$V_c(s) = \frac{b_c\widetilde{k}_p(s + \widetilde{k}_i/\widetilde{k}_p)}{s^2 + (a_c + b_c\widetilde{k}_p)s + b_c\widetilde{k}_i} V^*_c(s). \tag{12}$$

During the transient state, the gain $\widetilde{k}_p$ switches between $k_p^{av} + 2k_p^+$ and $k_p^{av} - 2k_p^+$. Upon reaching the steady state, $\widetilde{k}_p$ is kept constant at k_p^{av}. A similar statement applies to $\widetilde{k}_i$. Stability of the dc link is assured whenever

$$a_c + b_c\widetilde{k}_p > 0 \tag{13}$$

$$b_c\widetilde{k}_i > 0. \tag{14}$$

By using a suitable design procedure, these conditions can be easily fulfilled.

Define a sliding surface described by

$$\sigma = ce_v + \dot{e}_v \tag{15}$$

where $e_v = v^*_c - v_c$, $\dot{e}_v$ is its derivative, and c is a positive constant.

To prove the stability of the proposed $SM-PI$ at the origin $(\sigma = 0)$, let the Lyapunov candidate be

$$V(e_v) = \frac{1}{2}e_v^2. \tag{16}$$

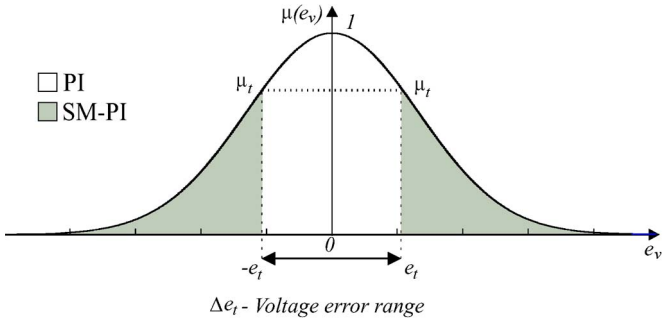


Fig. 5. Graph of the transition criterion μ.

Therefore, its time derivative can be expressed as

$$\dot{V}(e_v) = e_v \dot{e}_v = e_v(-ce_v) = -ce_v^2 < 0. \tag{17}$$

Since constant c is positive, the proposed control is asymptotically stable. Based on these stability restrictions, the controller gains can be determined by using the following switching laws:

$$\widetilde{k}_p = \left[(1+\text{sgn}(\sigma))\, k_p^+ - (1-\text{sgn}(\sigma))\, k_p^-\right] + k_p^{av} \tag{18}$$

$$\widetilde{k}_i = \left[(1+\text{sgn}(\sigma))\, k_i^+ - (1-\text{sgn}(\sigma))\, k_i^-\right] + k_i^{av} \tag{19}$$

where k_p^+, k_p^-, k_i^+, k_i^-, k_p^{av}, and k_i^{av} are positive constants determined as a function of the desired system performance (these gains can be obtained by using a standard PI design methodology, e.g., root locus). The mathematical function $\text{sgn}(\sigma)$ returns the values 1 for $\sigma > 0$ or -1 for $\sigma < 0$.

2) $DSM - PI$ Control Scheme: The $SM - PI$ controller has a good performance during the transient state but has an undesired side effect when the steady state is reached. It is the chattering originated by the SMC switching laws used for calculating the controller gains. This can be mitigated if the controller gains can be fixed in steady state (which results in a standard PI controller). It can be obtained by employing a transition rule in the controller structure. For this, consider a Gaussian function defined as

$$\mu(e_v) = e^{-\frac{e_v^2}{\lambda}} \tag{20}$$

where μ is the decision variable to select between the switching and fixed controllers, e_v is the dc-link voltage error, and λ is the parameter of the Gaussian function. Defining a range of values around the reference voltage of the dc link, i.e., Δe_t, it is possible to calculate the value of $\mu_t = \mu(e_t)$, from which the controller gains of $SM - PI$ are fixed (i.e., $\widetilde{k}_p = k_p^{av}$ and $\widetilde{k}_i = k_i^{av}$), as demonstrated in Fig. 5. In this graph, the value μ_t represents the threshold related to voltage error e_t where the controller transition must occur. Therefore, the transition works as follows: By using (20), the value of $\mu(e_v)$ is continuously calculated for each error voltage e_v. If this value is smaller than μ_t, the implemented controller is the $SM - PI$; otherwise, it is employed a standard PI with antiwindup (controller $SM - PI$ with fixed gains). To make this transition smooth, it is necessary to adequately adjust parameter λ. The higher λ, the less sensitive is μ to the voltage error e_v; otherwise, the smaller λ, the more sensitive will be μ to the voltage error e_v.

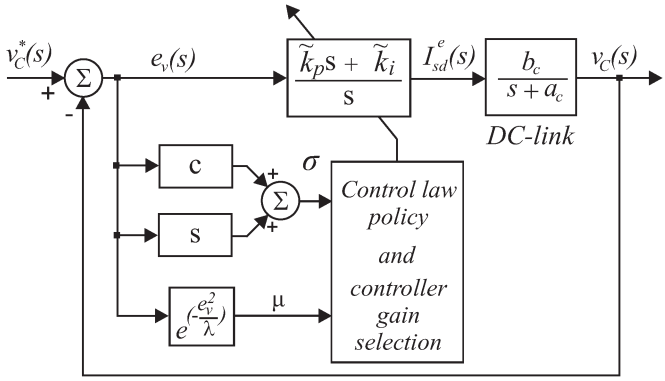


Fig. 6. Block diagram of the $DSM - PI$ control scheme. The $\widetilde{k}_p$ and $\widetilde{k}_i$ gains updating policy is as follows: for $\mu(e_v) < \mu_t$, the gains change according to (23) and (24), and for $\mu(e_v) \geqq \mu_t$, the gains are kept constant.

The block diagram of the proposed $DSM - PI$ controller is shown in Fig. 6. In which, the $DSM - PI$ controller gains $\widetilde{k}_p$ and $\widetilde{k}_i$ are determined by switching laws of (18) and (19) obtained from the sliding surface determined by blocks c and s.

3) Design Criteria of the $DSM - PI$: The design criterion employed in this paper is based in the pole assignment that requires the solution of the Diophantine equation. Thus, consider the transfer functions of dc link [see (3)] and the voltage regulator $DSM - PI$ [see (11)] can be written in terms of polynomials

$$G_v(s) = \frac{Z(s)}{R(s)} \tag{21}$$

$$C_c(v) = \frac{P(s)}{L(s)} \tag{22}$$

where $Z(s) = b_c$, $R(s) = s + a_c$, $P(s) = \widetilde{k}_p s + \widetilde{k}_i$, and $L(s) = s$. Then, the transfer function of the dc-link control loop will be given by

$$T_{et}(s) = \frac{Z(s)P(s)}{Z(s)P(s) + R(s)L(s)} \tag{23}$$

whose characteristic equation is

$$Z(s)P(s) + R(s)L(s) = 0. \tag{24}$$

The design objective is to find suitable polynomials $P(s)$ and $L(s)$ such that

$$Z(s)P(s) + R(s)L(s) = A^{\eta*}(s) \tag{25}$$

where $A^{\eta*}(s)$ is a desired harmonic Hurwitz polynomial, and superscript $\eta \in \{fs(\text{fast}), av(\text{average}), sl(\text{slow})\}$ refers to the performance criteria employed for determining desired polynomials. Once the suitable polynomials $A^{\eta*}(s)$ are defined, the voltage regulator parameters can be obtained from the solution of the Diophantine equation. The design criterion first determines the slow polynomial $(A^{sl*}(s))$ from the nominal parameters of the plant [see (3)], considering the performance indexes of maximum overshoot $M_p = 5\%$ and the damping coefficient of $\xi = 0.707$. Thus, the following polynomial can be obtained:

$$A^{sl*}(s) = s^2 + 2a_m^{sl} + 2\left(a_m^{sl}\right)^2 \tag{26}$$

TABLE I
SYSTEM PARAMETERS

$E_s = 110V(rms)$	$f_s = 60Hz$
$r_s = 0.2$	$l_s = 0.1mH$
$r_f = 2\Omega$	$l_f = 1mH$
$r_l = 40\Omega$	$l_l = 30mH$
$C = 2200\mu F$	$f_{sw} = 10kHz$

where $a_m^{sl} = 4/t_{ss(2\%)}^{sl}$, and $t_{ss(2\%)}^{sl} = t_{ss(2\%)}^{n}$ is the nominal settling time of system steady state. To determine the amplitudes of the switching laws given by (18) and (19), two other polynomials (i.e., $A^{av*}(s)$ and $A^{fs*}(s)$) are also defined, which correspond to a reduction of 40% and 62.5% of the nominal steady-state time $(t_{ss(2\%)}^{sl})$, respectively. Taking into account these three polynomials and solving the Diophantine equations for each case, the following gains can be obtained:

$$k_p^{\eta} = \frac{2a_m^{\eta} - a_c}{b_c} \tag{27}$$

$$k_i^{\eta} = \frac{2\left(a_m^{\eta}\right)^2}{b_c} \tag{28}$$

where k_p^{η} and k_i^{η}, with $\eta \in \{fs, av, sl\}$ referring to the controller gains obtained from the polynomials $A^{\eta*}(s)$. Therefore, it is possible to determine the coefficients k_p^+, k_p^-, k_i^+, and k_i^- as follows:

$$k_p^+ = \frac{k_p^{fs} - k_p^{av}}{2} \qquad k_i^+ = \frac{k_i^{fs} - k_i^{av}}{2} \tag{29}$$

$$k_p^- = \frac{k_p^{av} - k_p^{sl}}{2} \qquad k_i^- = \frac{k_i^{av} - k_i^{sl}}{2}. \tag{30}$$

IV. EXPERIMENTAL EVALUATION OF THE PROPOSED $SAPF$

The proposed control system presented in Fig. 4 has been experimentally evaluated by using a 10-kW three-phase active power filter laboratory prototype. It is composed by a three-phase power grid feeding a nonlinear load. The VSI is connected to the PCC by using input filter inductors $l_f = 1.0$ mH. The dc link is composed by capacitors of 2200 μF with a rated voltage of 410 V. The nonlinear load is implemented by a three-phase rectifier, feeding an RL load (i.e., $r_l = 40\ \Omega$ and $l_l = 30$ mH). The derivative of the load current reaches 16.32 kA/s, with total harmonic distortion $(THD) = 21.5\%$ and a lagging power factor of 0.89. The proposed control system was implemented on a $TMS283335$ DSP platform. The A/D converters of the DSP card are connected to a measurement unit, composed by Hall effect voltage and current sensors. The signal taken from these sensors passes through a first-order low-pass filter with cutoff frequency of $f_{\mathrm{LPF}} = 2.5$ kHz for antialiasing purposes. The control algorithm is implemented in C++ and executed with a sampling time of 100 μs. The $SAPF$ parameters of the laboratory prototype are provided in Table I.

Different conditions with hard transient and sudden load variations were considered in order to validate the theoretical studies developed in this manuscript. In addition, a comparison with a conventional PI controller was done to highlight the benefits of the proposed technique. The following scenarios were investigated: *a*) start-up charging the dc-link capacitor; *b*) transient of the dc-link reference voltage with both step-up and step-down variations; *c*) hard load transient variation by increasing and reducing the load power; *d*) unbalanced grid voltage; and finally *e*) reactive power compensation.

The parameters of the $DSM - PI$ controller employed in the experimental tests are presented in Table II.

TABLE II
$DSM - PI$ CONTROLLER PARAMETERS

$k_p^+ = 0.033$	$k_p^- = 0.022$	$k_p^{av} = 0.11$
$k_i^+ = 2.145$	$k_i^- = 0.88$	$k_i^{av} = 2.75$
$c = 100$	$\lambda = 500$	$\mu_t = 0.98$

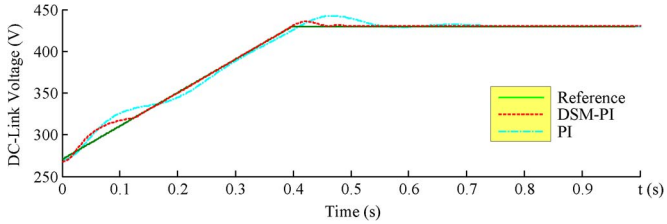


Fig. 7. Experimental result for dc-link voltage v_C during startup.

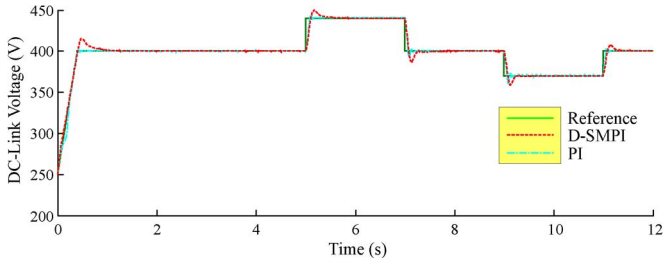


Fig. 8. Experimental result for dc-link voltage v_C during step transient of its reference voltage with both step-up and step-down variations.

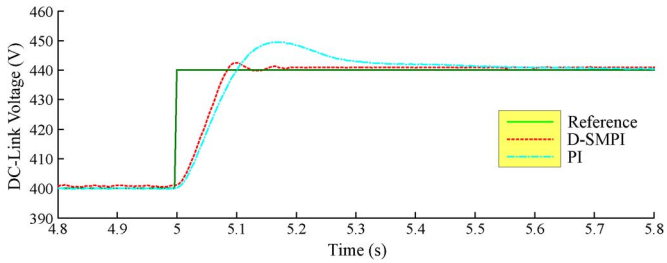


Fig. 9. Experimental result for dc-link voltage v_C during step transient of its reference voltage.

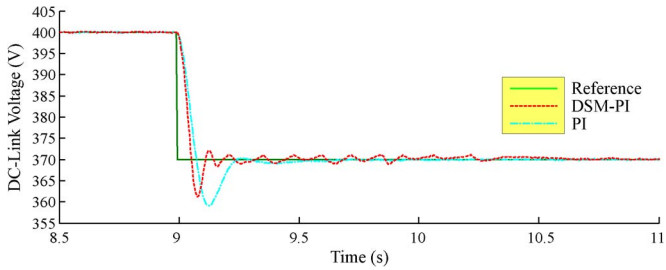


Fig. 10. Experimental result for dc-link voltage v_C during step transient of its reference voltage.

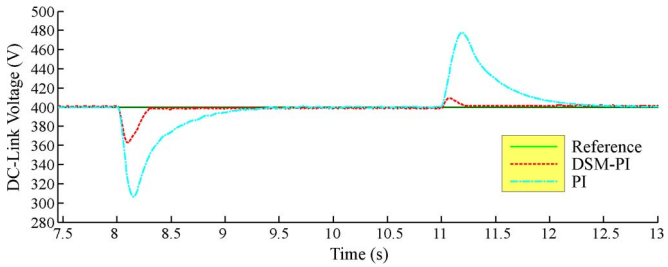


Fig. 11. Experimental result for dc-link voltage (v_c) during load transients.

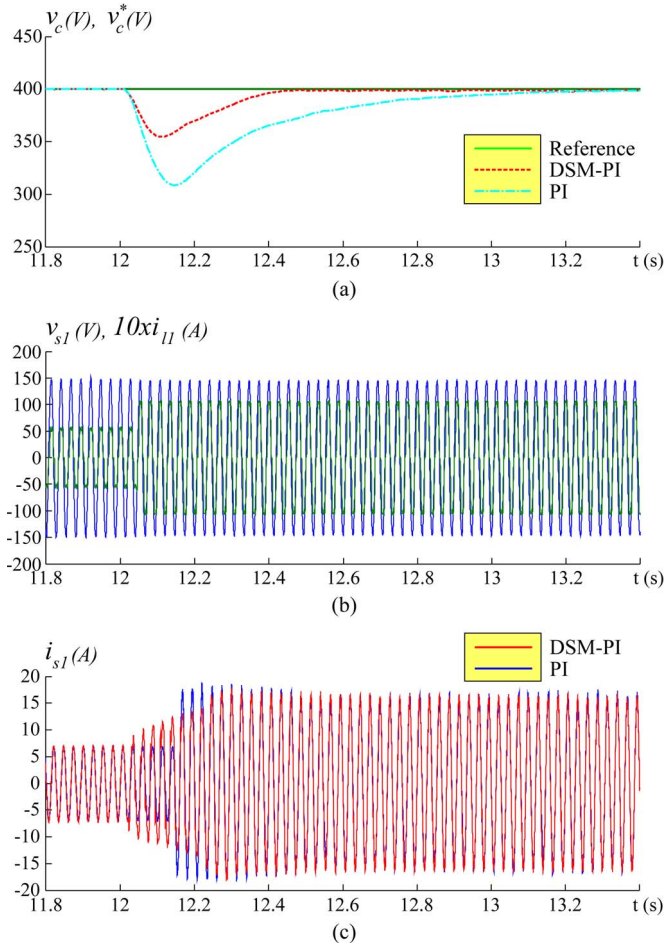


Fig. 12. Experimental result during load transients (a) for dc-link voltage v_c, (b) for source voltage v_{s1} and the load current i_{l1} multiplied by 10 times, and (c) for source current i_{s1}.

As aforementioned, the first test employed to verify and compare the controllers was the starting-up procedure for the dc-link voltage. Fig. 7 depicts the experimental outcome comparing both controllers following a reference ramp. Such a ramp waveform has a slope of 347 V/s. Notice in Fig. 7 that the performance of the proposed converter is smoother and the response time is smaller; the overshoot values of the proposed and conventional converters are given respectively by 0.53% and 4.37%.

Although the comparison shown in Fig. 7 brings up the benefits of the $DSM - PI$ strategy, additional tests have been considered to highlight its advantage under operating regimes.

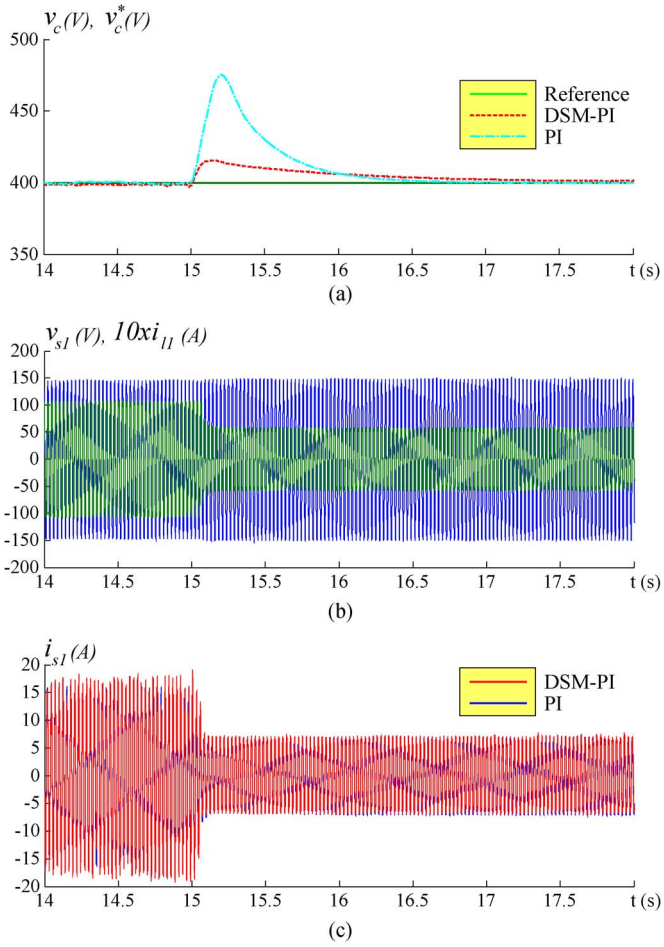


Fig. 13. Experimental result during load transients (a) for dc-link voltage v_c, (b) for source voltage v_{s1} and the load current i_{l1} multiplied by 10 times, and (c) for source current i_{s1}.

For instance, Fig. 8 presents a comparison for both controllers for variations of the dc-link reference voltage. The proposed approach $(DSM - PI)$ performed better for all step transients (either step up or step down) presented in this figure. A zoom of the transient at $t = 5$ s is presented in Fig. 9, whereas Fig. 10 shows a zoom of the step-down transient at $t = 9$ s. Even assuming that the results presented in Figs. 8–10 do not represent a practical need for active power filters, those results are important figures of merit to show the advantages of the proposed controllers.

On the other hand, Figs. 11–13 show a typical type and ever-present transient in active power filter applications, i.e., transitory of load power. Two types of variations are considered; the first one (see Fig. 12) at $t = 12$ s shows the load power increase with an additional three-phase resistor (30 Ω) connected in parallel with the arrangement of linear and nonlinear loads.

For this load transient, the parameters of the controllers are given as follows: 1) conventional PI, undershoot: 22.9% and accommodation time (2%): 0.84 s; and 2) proposed $DSM - PI$, undershoot: 11.35% and accommodation time (2%) 0.344 s. The $DSM - PI$ controller also performs better than the conventional approach with load power reduction (see Fig. 13), as observed at $t = 15$ s. Such a transient was obtained by disconnecting the resistive load.

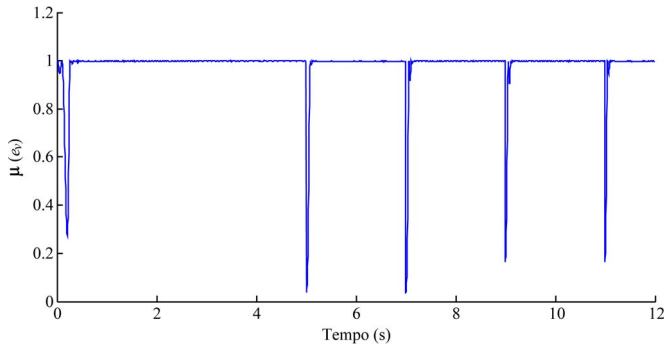


Fig. 14. Experimental result for function μ used for commutation between the controllers PI and $DSM - PI$.

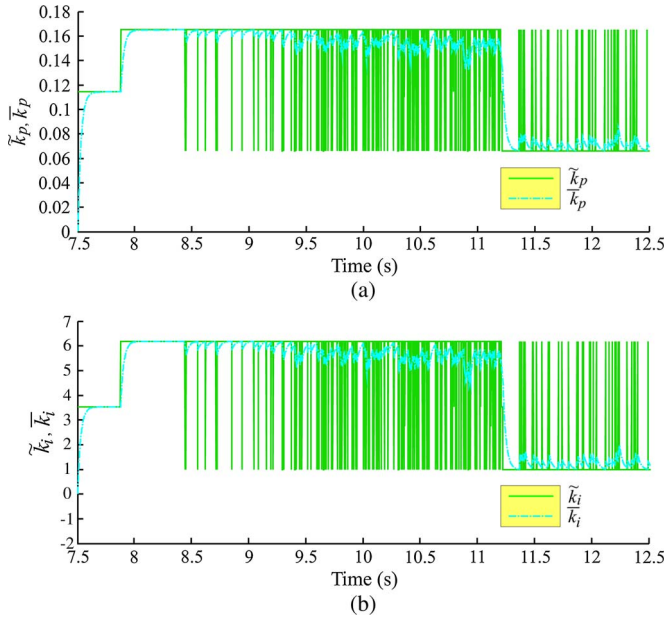


Fig. 15. Experimental result (*a*) for switching proportional gain $\widetilde{k}_p$ and its average value $\overline{k}_p$ and (*b*) for the switching integral gain $\widetilde{k}_i$ and its respective average value $\overline{k}_i$ during load transient.

It is evident that the transition function of the proposed controller [see (20)] plays an important role to improve the performance of the dc-link voltage control. Fig. 14 shows the behavior of $\mu(e_v)$ for the results presented in Fig. 8.

Fig. 15 shows, in turn, the gains behavior for the results in Fig. 11, in which switching gains of the controllers and their average values can be observed. Notice that they have been adapted during the load transient. Fig. 16 shows another set of experimental outcomes to stress the gains behavior through the start-up charging of the dc-link capacitor voltage.

Figs. 17–19 show the oscilloscope screenshots with the results for the case where unbalanced voltages were obtained at the grid side, as observed in Fig. 17. Figs. 18 and 19 show load and grid currents, respectively. Notice that even assuming this case, the active power filter with $DSM - PI$ controller operates as expected. This can be also observed when the $THDs$ before and after the compensation are evaluated, as shown in the frequency spectra of grid phase current i_{s1} presented in Fig. 20. After the compensation implemented by the $SAPF$, the harmonic distortion is $THD \simeq 3.6\%$.

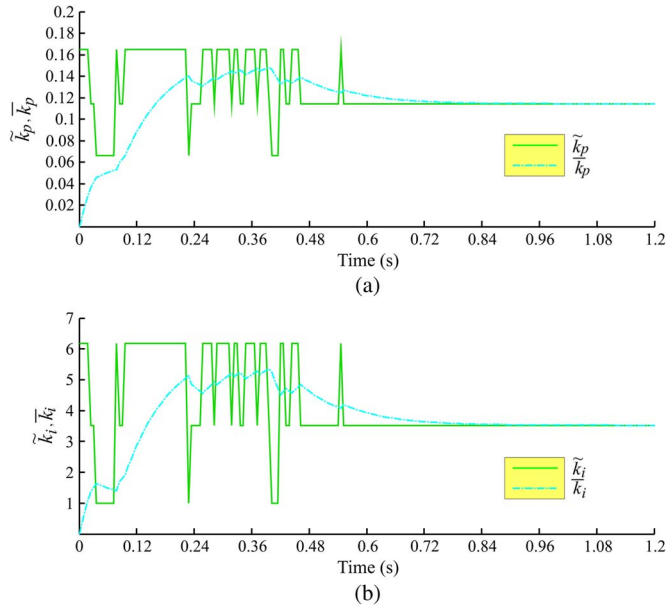


Fig. 16. Experimental result (*a*) for switching proportional gain $\widetilde{k}_p$ and its average value $\overline{k}_p$ and (*b*) for the switching integral gain $\widetilde{k}_i$ and its respective average value $\overline{k}_i$ during start-up charging of the dc-link capacitor.

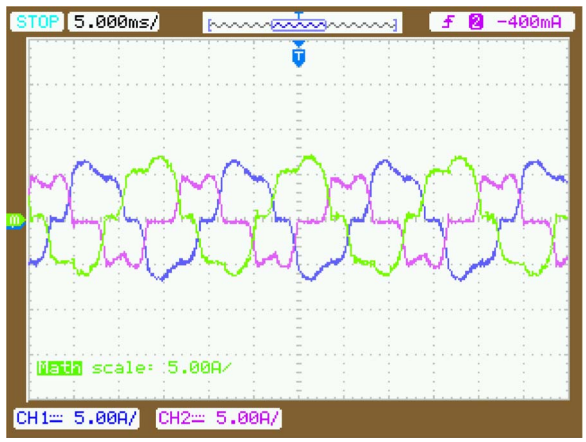


Fig. 17. Experimental results of the grid phase currents under unbalanced grid phase voltages before the compensation scheme.

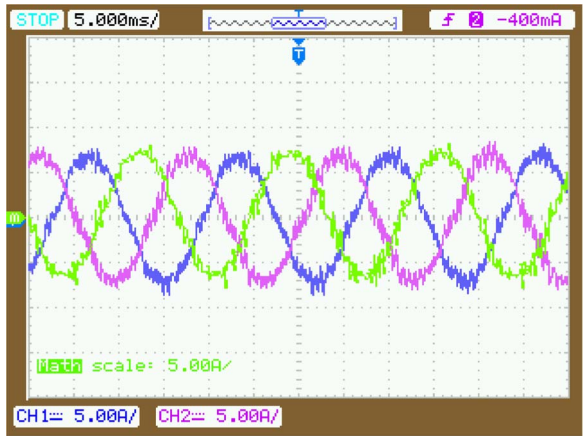


Fig. 18. Experimental result of the grid phase currents under unbalanced conditions of grid after the compensation scheme.

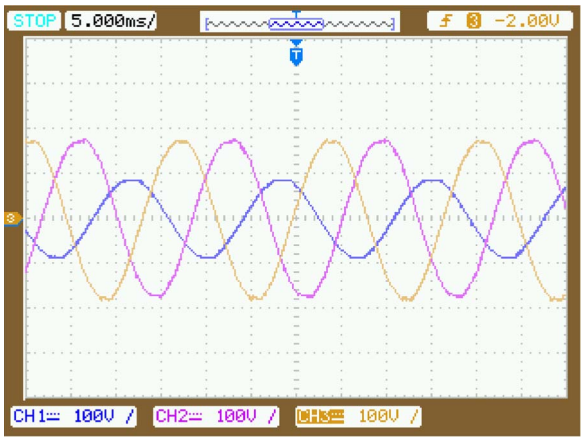


Fig. 19. Experimental result of unbalanced grid phase voltages.

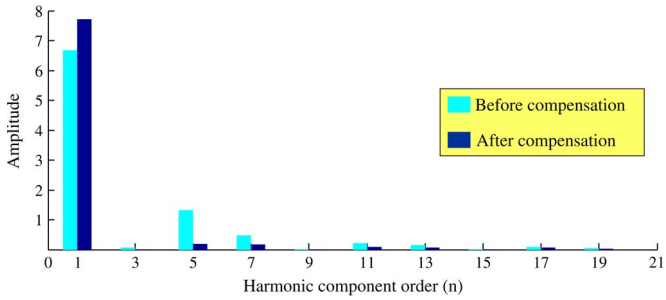


Fig. 20. Frequency spectra of the grid phase current i_{s1} before and after the compensation scheme.

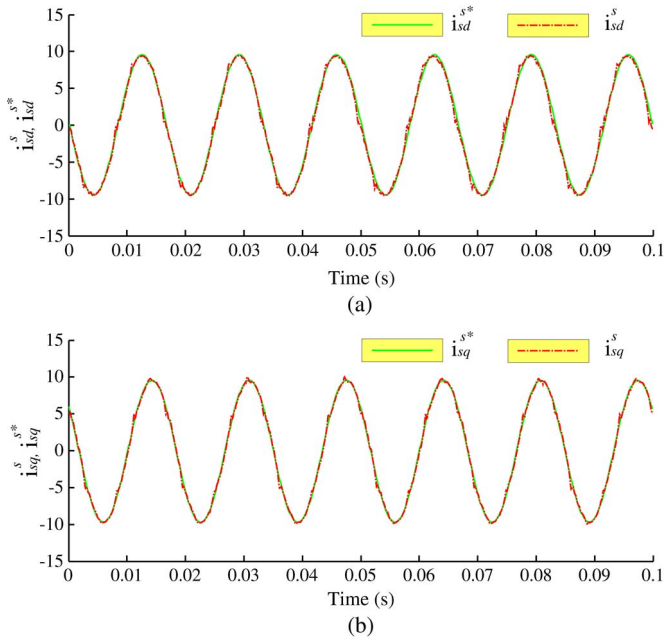


Fig. 21. Experimental result for the controlled current i^s_{sdq} in the dq reference frame.

Fig. 21 shows the steady-state results highlighting the current control actions with the measured dq currents following their reference.

The performance of the $SAPF$ when the reactive power is compensated can be verified in Figs. 22 and 23. Fig. 22 presents the experimental result of the grid phase voltage v_{s1}

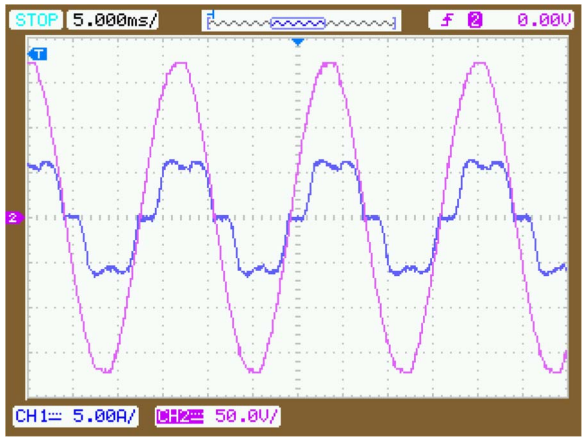


Fig. 22. Experimental result of the grid phase voltage v_{s1} superimposed by grid phase current i_{s1} before the compensation.

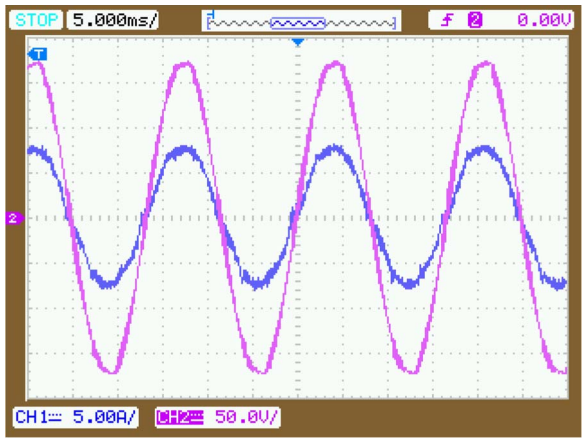


Fig. 23. Experimental result of the grid phase voltage v_{s1} superimposed by grid phase current i_{s1} after the compensation.

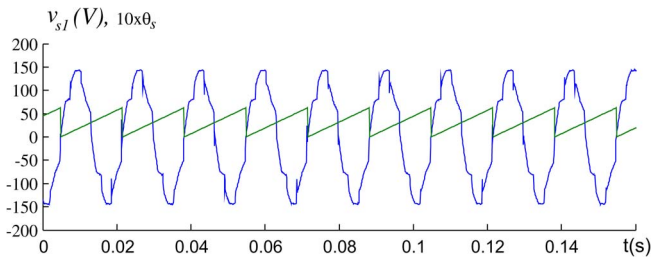
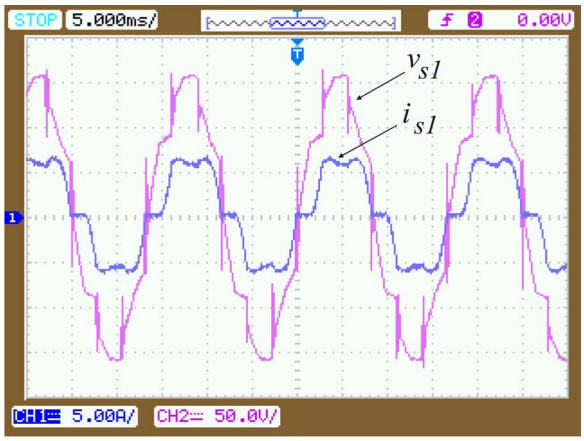


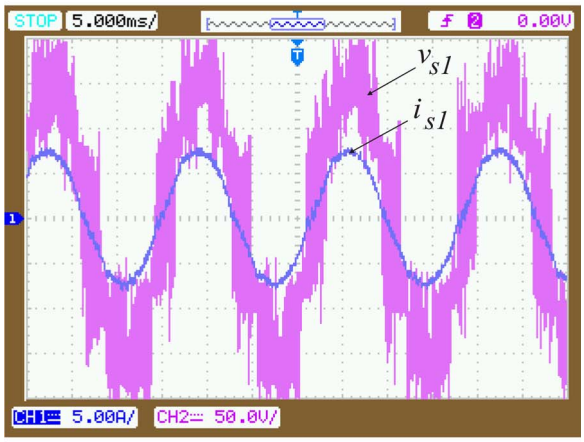
Fig. 24. Experimental result for distorted source voltage v_{s1} and the respective PLL angle.

superimposed by its grid phase current i_{s1} before enabling the compensation scheme. Fig. 23 presents the same graphs when the compensation is effected by the $SAPF$. The last experimental result demonstrates that the reactive power demanded by the nonlinear load is full compensated.

Figs. 24 and 25 present experimental results for the $SAPF$ under distorted source voltage. In Fig. 24, it is possible to verify the source voltage V_{s1} and its respective PLL angle θ_s. Fig. 25 presents the source voltage v_{s1} and the respective source current i_{s1} before and after compensation imposed by $SAPF$.



(a)



(b)

Fig. 25. Experimental result for distorted source voltage v_{s1} and the source current i_{s1} (a) before and (b) after $SAPF$ compensation.

V. Conclusion

This paper has proposed a control approach for improving the performance of $SAPF$ without load current measurements. In this control approach, the dc-link voltage is regulated by a dual control scheme implemented by proportional–integral (PI) controller with the gains calculated by using an SMC approach. The chattering due to the SM can be mitigated by using a transition rule in the controller structure. The theoretical bases of the $SM-PI$ was introduced, and the stability proof was presented. Moreover, the transition scheme that results in $DSM-PI$ was also discussed. With this control strategy, the performance of the dc-link control loop during the load variations is enhanced. The phase currents of the power grid are indirectly regulated by two independent controllers $(DSCs)$, in which the IMP is employed to avoid reference frame transformations. This demonstrates that there are significant gains in the $SAPF$ based on the $BEBS$ since the current control strategy is simpler and the filter control strategy is implemented with reduced number of current sensors. A comprehensive set of experimental results demonstrates the effectiveness of the proposed control strategy even during system load variation while providing simultaneously system reactive power compensation and harmonic mitigation.

References

[1] IEC 60601-1, International Electrotechnical Commission, Geneva, Switzerland. Rep. CEI/IEC 60601-1: 1988, 1988.
[2] *Draft Guide for Applying Harmonic Limits on Power Systems*, IEEE Std. P519.1/D12 2012.
[3] H. Akagi, "Trends in active power line conditioners," *IEEE Trans. Power Electron.*, vol. 9, no. 3, pp. 263–268, May 1994.
[4] B. Singh and V. Verma, "Selective compensation of power-quality problems through active power filter by current decomposition," *IEEE Trans. Power Del.*, vol. 23, no. 2, pp. 782–799, Apr. 2008.
[5] B. Singh, K. Al-Haddad, and A. Chandra, "A review of active filters for power quality improvements," *IEEE Trans. Ind. Electron.*, vol. 46, no. 5, pp. 960–971, Oct. 1999.
[6] F. A. S. Neves, H. E. P. de Souza, M. C. Cavalcanti, F. Bradaschia, and E. J. Bueno, "Digital filters for fast harmonic sequence component separation of unbalanced and distorted three-phase signals," *IEEE Trans. Ind. Electron.*, vol. 59, no. 10, pp. 3847–3859, Oct. 2012.
[7] M. Angulo, J. Lago, D. Ruiz-Caballero, S. Mussa, and M. Heldwein, "Active power filter control strategy with implicit closed loop current control and resonant controller," *IEEE Trans. Ind. Electron.*, vol. 6, no. 7, pp. 2721–2730, Jul. 2013.
[8] A. Bhattacharya and C. Chakraborty, "A shunt active power filter with enhanced performance using ANN-based predictive and adaptive controllers," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 421–428, Feb. 2011.
[9] S. Bhattacharya, T. M. Frank, D. M. Divan, and B. Banerjee, "Active filter system implementation," *IEEE Ind. Appl. Mag.*, vol. 4, no. 5, pp. 47–63, Sep./Oct. 1998.
[10] F. Z. Peng, G. W. Ott, Jr., and D. J. Adams, "Harmonic and reactive power compensation based on the generalized instantaneous reactive power theory for three phase four wire system," *IEEE Trans. Power Electron.*, vol. 13, no. 6, pp. 1174–1181, Nov. 1998.
[11] R. Pereira, C. da Silva, L. da Silva, and G. Lambert-Torres, "New strategies for application of adaptive filters in active power filters," *IEEE Trans. Ind. Appl.*, vol. 47, no. 3, pp. 1136–1141, May/Jun. 2011.
[12] M. Forghani and S. Afsharnia, "Online wavelet transform-based control strategy for UPQC control system," *IEEE Trans. Power Del.*, vol. 22, no. 1, pp. 481–491, Jan. 2007.
[13] P. Kumar and A. Mahajan, "Soft computing techniques for the control of an active power filter," *IEEE Trans. Power Del.*, vol. 24, no. 1, pp. 452–461, Jan. 2009.
[14] M. Qasin, P. Kanjiya, and V. Khadkikar, "Artificial-neural-network-based phase-locking scheme for active power filters," *IEEE Trans. Power Electron.*, vol. 61, no. 8, pp. 3857–3866, Aug. 2014.
[15] J. C. Wu and H. L. Jou, "Simplified control method for the single-phase active power filter," *Proc. Inst. Elect. Eng.— Elect. Power Appl.*, vol. 143, no. 3, pp. 219–224, May 1996.
[16] T. E. Nunez-Zuniga and J. A. Pomilio, "Shunt active power filter synthesizing resistive load," *IEEE Trans. Power Electron.*, vol. 17, no. 2, pp. 273–278, Mar. 2002.
[17] R. Ribeiro, C. Azevedo, and R. Sousa, "A robust adaptive control strategy of active power filters for power-factor correction, harmonic compensation, and balancing of nonlinear loads," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 718–730, Feb. 2012.
[18] Z. Chen, Y. Luo, and M. Chen, "Control and performance of a cascaded shunt active power filter for aircraft electric power system," *IEEE Trans. Ind. Electron.*, vol. 59, no. 9, pp. 3614–3623, Sep. 2012.
[19] Q. Trinh and H. Lee, "An advanced current control strategy for three-phase shunt active power filter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 12, pp. 5400–5410, Sep. 2013.
[20] W. Longhui, Z. Fang, Z. Pengbo, L. Hongyu, and W. Zhaoan, "Study on the influence of supply-voltage fluctuation on shunt active power filter," *IEEE Trans. Power Del.*, vol. 22, no. 3, pp. 1743–1749, Jul. 2007.
[21] C.-S. Lam, W.-H. Choi, M.-C. Wong, and Y.-D. Han, "Adaptive dc-link voltage-controlled hybrid active power filters for reactive power compensation," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1758–1772, Apr. 2012.
[22] M. J. Newman, D. N. Zmood, and D. G. Holmes, "Stationary frame harmonic reference generation for active filter systems," *IEEE Trans. Ind. Appl.*, vol. 38, no. 6, pp. 1591–1599, Nov./Dec. 2002.
[23] X. Yuan, W. Merk, S. Stemmler, and J. Allmeling, "Stationary-frame generalized integrators for current control of active power filters with zero steady-state error for current harmonics of concern under unbalanced and distorted operating conditions," *IEEE Trans. Ind. Appl.*, vol. 38, no. 2, pp. 523–532, Mar./Apr. 2002.

[24] L. Malesani, P. Matavelli, and S. Buso, "Robust dead-beat current control for PWM rectifiers and active filters," *IEEE Trans. Ind. Applicat.*, vol. 35, no. 3, pp. 613–620, May/Jun. 1999.
[25] J. Matas, L. Vicuna, J. Guerrero, and M. Castilla, "Feedback linearization of a single-phase active power filter via sliding mode control," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 116–125, Jan. 2008.
[26] K.-K. Shyu, M.-J. Yang, Y.-M. Chen, and Y.-F. Lin, "Model reference adaptive control design for a shunt active-power-filter system," *IEEE Trans. Ind. Electron.*, vol. 55, no. 1, pp. 97–106, Jan. 2008.
[27] H. Yi, F. Zhuo, Y. Zhang, Y. Li, W. Chen, and J. Liu, "A source-current-detected shunt active power filter control scheme based on vector resonant controller," *IEEE Trans. Ind. Appl.*, vol. 50, no. 3, pp. 1953–1965, May–Jun. 2014.
[28] D. Chen, J. Zhang, and Z. Qian, "An improved repetitive control scheme for grid-connected inverter with frequency-adaptive capability," *IEEE Trans. Ind. Electron.*, vol. 60, no. 2, pp. 814–823, Feb. 2013.
[29] C. Lascu, L. Asiminoaei, I. Boldea, and F. Blaabjerg, "Frequency response analysis of current controllers for selective harmonic compensation in active power filters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 337–347, Feb. 2009.
[30] M. Gasperi, "Life prediction modeling of bus capacitors in ac variable-frequency drives," *IEEE Trans. Ind. Appl.*, vol. 41, no. 6, pp. 1430–1435, Nov./Dec. 2005.
[31] A. Braham, A. Lahyani, P. Venet, and N. Rejeb, "Recent developments in fault detection and power loss estimation of electrolytic capacitors," *IEEE Trans. Power Electron.*, vol. 25, no. 1, pp. 33–43, Jan. 2010.
[32] C. Jacobina, M. Correa, R. Pinheiro, E. da Silva, and A. Lima, "Modeling and control of unbalanced three-phase systems containing PWM converters," *IEEE Trans. Ind. Appl.*, vol. 37, no. 6, pp. 1807–1816, Nov./Dec. 2001.

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